(c) forming a first upper layer comprising a material different from the first conductive layer on the first conductive layer;

(d) forming a second upper layer comprising a material different from the first upper layer on the first upper layer;

(e) forming sidewall spacers on side walls of the first conductive layer, the first upper layer and the second upper layer;

B2 (f) forming an insulation layer that covers the second upper layer and the sidewall spacers;

(g) planarizing the insulation layer until an upper surface of the second upper layer is exposed;

(h) removing the second upper layer;

(i) removing the first upper layer to form a recessed section between the sidewall spacers; and

(j) forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer.

B3 3. (amended) A method for manufacturing a semiconductor device according to claim 1, wherein the step (i) is conducted by an etching method, and in the step (i), a ratio of an etching rate of the first upper layer with respect to an etching rate of the first conductive layer is two or greater.

5. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising, after step (i), forming a barrier layer between the first conductive layer and the second conductive layer.

B4 6. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising, after step (i), forming a barrier layer between the first conductive layer and the second conductive layer, and forming the barrier layer between the second conductive layer and the sidewall spacers.

7. (amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer;

(b) forming a first conductive layer on the gate dielectric layer;

(c) forming an upper layer on the first conductive layer, at least a lower portion of the upper layer comprising a material different from at least an upper portion of the first conductive layer;

(d) forming sidewall spacers on side walls of the first conductive layer and the upper layer;

(e) forming an insulation layer that covers the upper layer and the sidewall spacers;

(f) planarizing the insulation layer until an upper surface of the upper layer is exposed;

(g) removing the upper layer to form a recessed section between the sidewall spacers on the upper portion of the first conductive layer; and

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(h) forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer.

8. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the step (g) is conducted by an etching method, and in the step (g), a ratio of an etching rate of at least the lower portion of the upper layer with respect to an etching rate of the at least upper portion of the first conductive layer is two or greater.

9. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the first conductive layer is formed from a polysilicon layer.

10. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the second conductive layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.

11. (amended) A method for manufacturing a semiconductor device according to claim 7, further comprising, after step (g), forming a barrier layer between the first conductive layer and the second conductive layer.

12. (amended) A method for manufacturing a semiconductor device according to claim 7, further comprising, after step (g), forming a barrier layer between the first conductive layer and the second conductive layer, and forming the barrier layer between the second conductive layer and the sidewall spacers.

13. (amended) A method for manufacturing a semiconductor device, the method comprising:

forming a gate dielectric layer;

forming a first conductive layer on the gate dielectric layer;

B4 forming an upper layer on the first conductive layer, the upper layer comprising a material different from that of the first conductive layer;

forming sidewall spacers on side walls of the first conductive layer and the upper layer;

removing the upper layer to form a recessed section between the sidewall spacers and above at least part of the first conductive layer; and

forming a second conductive layer in the recessed section to form a gate electrode comprising the at least part of the first conductive layer and the second conductive layer.

14. (amended) A method for manufacturing a semiconductor device according to claim 13, further comprising, after the removing the upper layer and prior to forming the second conductive layer, forming a barrier layer on the first conductive layer.

15. (amended) A method for manufacturing a semiconductor device according to claim 13, further comprising, after the removing the upper layer and prior to the forming a second conductive layer, forming a barrier layer on the first conductive layer and the sidewall spacers, wherein the barrier layer will be positioned between the first conductive layer and the second conductive layer and between the sidewall spacers and the second conductive layer.

16. (amended) A method for manufacturing a semiconductor device according to claim 13, wherein the first conductive layer and second conductive layer comprises materials having different compositions.

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17. (amended) A method for manufacturing a semiconductor device according to claim 13, wherein the first conductive layer comprises polysilicon and the second conductive layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.

Please add new claims 22-26 as follows:

--22. (new) A method for manufacturing a semiconductor device according to claim 1, wherein the second upper layer and the first conductive layer are formed from an identical material.

23. (new) A method for manufacturing a semiconductor device according to claim 1, wherein the second upper layer and the first conductive layer each comprise polysilicon.

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24. (new) A method for manufacturing a semiconductor device according to claim 7, further comprising forming the upper layer to include an upper portion, and wherein the upper portion and the first conductive layer are formed from an identical material.

25. (new) A method for manufacturing a semiconductor device according to claim 14, further comprising:

forming the first conductive layer from a material comprising polysilicon,

forming the upper layer to include a lower portion formed from silicon nitride and an upper portion formed from polysilicon, and

forming the second conductive layer from a material selected from the group consisting of a metal, a metal alloy, and a metal compound.